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LARGER ARRAY FINE PITCH WAFER LEVEL PACKAGE DROP TEST RELIABILITY

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ABSTRACT

In this study, drop test reliabilities of wafer level packages (WLP) are investigated. Failure mechanism, crack map and crack initiation location are presented. Failure rates of six groups defined by JEDEC are examined through both drop test experiment and finite element (FE) analysis with ANSYS software. Effects of component placement, PCB design, WLP structures, array size, pitch, and solder alloy are studied through drop test experiment per JESD22-B111 and finite element modeling.

It is found that the primary failure mechanism of WLP drop test failures is fracture of intermetallic compound (IMC) at WLP side. During the drop test, solder joints at outer columns experience most stress and will fracture first. And the corner balls always fail first. The crack initiates at inner side of solder joint and propagates to the opposite side. When JEDEC recommended PCB is used for WLP drop test, the corner components fail first. This is different from the findings from BGA packages. It is confirmed that the dominant failure rate of corner WLP components is mainly due to the effect of mounting screws, rather than the intrinsic drop test reliability of WLP. Therefore, it is not appropriate to judge the drop test reliability of WLP with the drop test data for the corner components. Instead, middle component drop test data represent intrinsic shock resistance of WLP, and they should be used to represent the drop test performance of WLP.

Drop test DOE results showed that WLP structure and material make visible difference. Non-soldermask defined (NSMD) PCB pad designs result in better drop reliability than SMD pads. With a given ball array, WLP with smaller pitch has worse drop reliability. As array size increases, the drop test performance drops significantly. In addition, choice of solder alloy makes visible difference for WLP.

INTRODUCTION

Wafer level packages are increasingly accepted in portable electronics due to its small form factors and low manufacturing cost. Larger array and finer pitch WLP are needed to allow the increased functionality while keeping small footprint. Drop test performance has been the key package reliability indicator for portable applications. JEDEC has published a test standard[1] with detailed test procedures and board design for board level drop test of components used in handheld electronic products. Much work has been done to address the drop test performance of BGA packages[2]-[7]. Effects of thermal aging on BGA drop test performance are also studied[8]&[9]. The failure mechanism and effect of solder alloy choices on BGA drop reliabilities are well understood. Finite Element (FE) modeling methodologies for drop test are introduced by various researchers[10]-[15]. Recent studies in WLP drop test reliability have been published[16]-[21]. They include drop test at room and elevated temperatures. Anderson et al[10] and Tee et al[20] studied the risk of drop test failure due to PCB trace crack. It was concluded that with optimized PCB layout to avoid trace crack, drop test reliability of the WLP considered well exceeds the requirement. Dhiman et al[14] discovered through FE modeling that WLP's next to mounting screws always failed first. This study concluded that the corner WLP failures are due to effect of mounting screws, not intrinsic strength of WLP. As result of this study, a modified test board is proposed to eliminate the corner component failure due to mounting screws. Additional drop test studies can be found in the literature[22]-[28].

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In this work, large array and fine pitch WLP drop test data are examined through drop test and FE modeling with ANSYS software. The drop test method is specified by JESD22-B111[1]. The methodology of drop test modeling with FE is described in previous work[13]. In the following sections, overall failure rates of different component groups are presented. Effect of mounting screws is investigated and a criterion for WLP drop test reliability comparison was established. Failure mechanism, crack map after drop test, crack initiation and its propagation are investigated through failure analysis (FA) and FE modeling. Effect of design and material parameters are then studied. These parameters include: PCB pad design, WLP structures, array size, ball pitch, and solder ball alloy. Conclusions are made at the end.

NOMENCLATURE

WLP: Wafer Level Package
FFT: Fast Fourier Transform
IMC: Intermetallic Compound
BGA: Ball Grid Array

JEDEC DROP TEST FOR WLP

According to JESD22-B111[1], a 132x77 mm 8 layer PCB is defined for drop test. The JEDEC method recommends mounting 15 components on the board in 3 rows of 5 components. This is illustrated in Figure 1. According to the standard, all components must be located within the 95 mm X 61 mm box. The outer edges of out side components (U1 through U6 and U10 through U15) shall align with the boundary of this box, guaranteeing a fixed diagonal distance of (4 mm) between the outside of screw head and component's corner closest to the screw head (components U1, U3, U5, U11, U13, and U15) irrespective of component size. Based on symmetry, the 15 components are classified in five groups (A – F in Figure 1). The component locations for a WLP with body size <15 mm are illustrated in Figure 2. The board is mounted on a base plate by using four screws at the corners. This base plate is then mounted on a drop table. The drop table, guided by guide rods, is allowed to strike on a rigid base from a specified height. A half sine-impulse is produced when the table strikes the rigid base. JEDEC condition B is used for this study. The input acceleration of this condition is 1500 g peak and 0.5 ms duration measured on base plate.

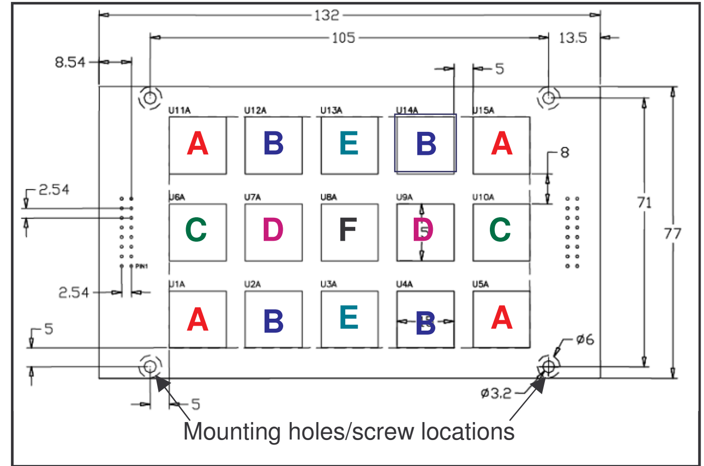

Figure 1. JEDEC drop test board outline and component location.

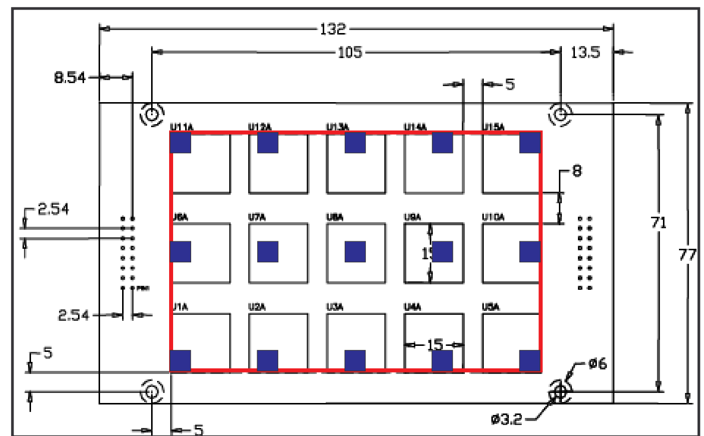

Figure 2. WLP component locations per JESD22-B111. Blue squares represent WLP, red box defines the edges of outer components.

Drop tests analyses have shown that the primary failure mechanism for the WLP considered is fracture of IMC at WLP side. Solder joint maximum peeling stress is used to determine the risk of solder joint fracture during drop test. During drop test, the PCB vibrates. The stress status of corner solder joints is illustrated by Figure 3. When the PCB bends downwards, the solder joint is distorted resulting in tensile stress at point B and C while compressive stress at A and D. When the PCB bends upwards, the stress signs are reversed. Therefore, during drop test solder joint cracks may develop from both sides of the solder joint, inner side and outer side. Here inner side is closer to package center.

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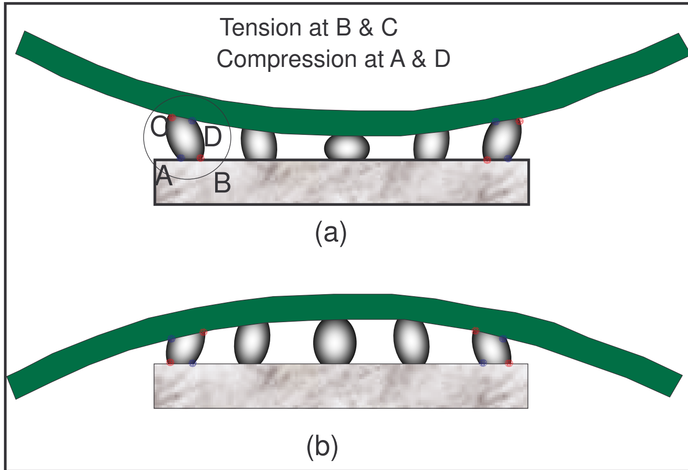
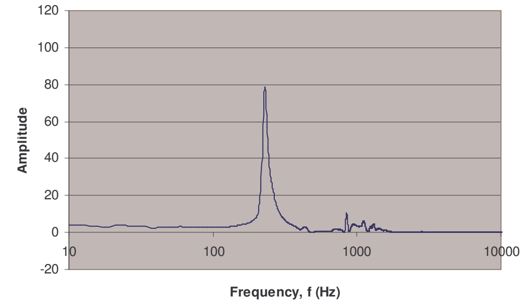


Figure 3. Illustration of solder joint stress during drop test. (a) PCB bends downwards, and (b) PCB bends upwards. Red dots mark the location with tensile stress and blue points show the location with compressive stress.

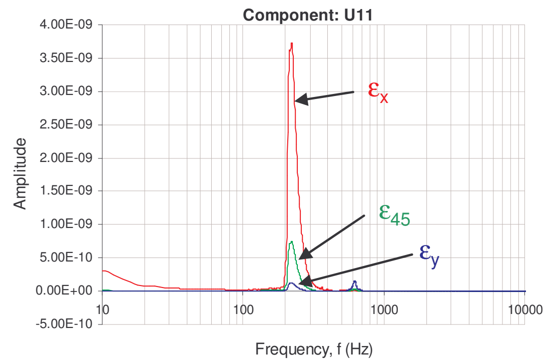
Frequency analysis

Frequency analysis of PCB vibration is presented to better explain observation from drop tests. Accelerometers and strain gages are mounted to PCB. PCB acceleration and strains as functions of time are obtained with NI CompactDAQ data acquisition system. The frequency spectra are generated by performing fast Fourier transform (FFT) with MATLAB software. Figure 4 shows the frequency spectra of PCB acceleration and strains. First of all, an accelerometer is mounted on top of group F component. The acceleration is measured after a metal object hits the board (generates white noise incidence). The acceleration spectrum at group F component is plotted in 4 (a). Here the resonant frequency correlates the first acceleration peak at the spectrum. The resonance frequency thus measured is 230 Hz. PCB strains at three directions are measured next to group A, F and C components. The PCB strain spectra are shown in 4 (b), (c) and (d) for these three components, respectively. As is seen the first resonant frequency is registered at 230 Hz. And second one is found at ~ 650 Hz for group C. It is observed that the PCB strains for groups A and F are ε_x dominant, while it is ε_y dominant for group C.

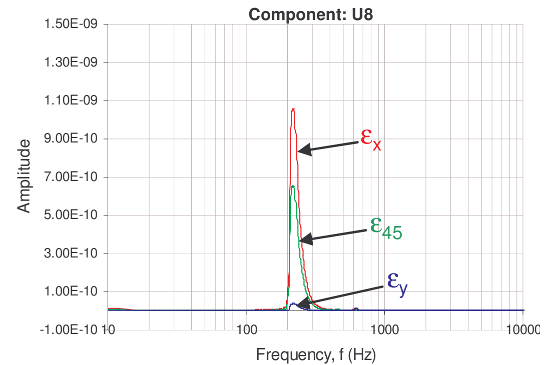
In order to better understand these observations, the Eigen value problem is solved with FE modeling for JEDEC drop test board. The first two symmetrical modes are shown in Figure 5. The corresponding natural frequencies are 220 Hz and 654 Hz, respectively. It is seen that at fundamental frequency, the mode shape is ε_x dominant. While at 654 Hz the mode shape is ε_y dominant. Modeling results correlate very well with measured data (Figure 4).



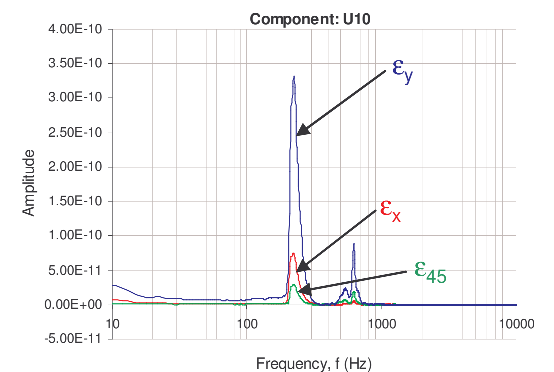
(a) Acceleration



(b) Group A



(c) Group F



(d) Group[C

Figure 4. Frequency spectra for PCB acceleration and strains. (a) Acceleration spectrum upon white noise incidence, (b) strain spectra for group A, (c) strain spectra at group G, and (d) strain spectra at group C.

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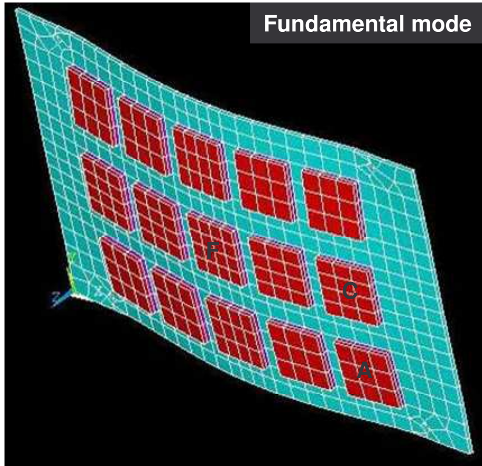
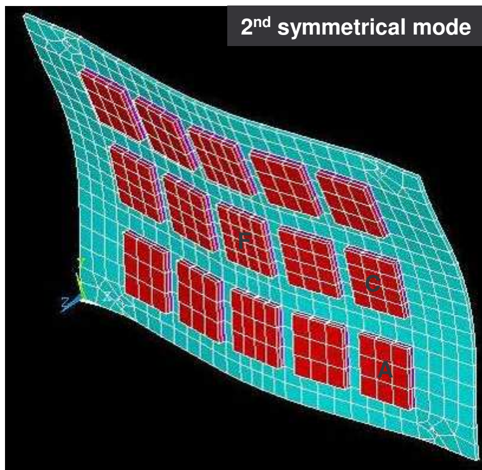


(a)



(b)

Figure 5. Natural frequency and mode shapes calculated with FE modeling. (a) Fundamental mode. Natural frequency is f_0 = 220 Hz. The vibration is ε_x dominant. (b) Next symmetrical mode. Natural frequency is f_1 = 654 Hz. The vibration is ε_y dominant.

JEDEC drop test analysis

FE modeling is performed for 0.5 mm pitch 12x12 and 6x6 arrays WLP during drop test per JEDEC condition B. The peeling stress distribution at IMC layer of the 12x12 array WLP group A components are shown in Figure 6. It is seen that the solder joints on left most and right most columns experience higher peeling stress than other columns. The lower left corner solder joint sees the highest stress among all solder joints. In addition, the maximum stress is at inner side of the solder joint. Here the inner side is towards the die center. This suggests that the primary crack initiate from inner side of the solder joint. To verify these observations, failure analysis of a group A WLP is done with dye&pry. The crack size and locations are illustrated in Figure 7. It is seen from this Figure that the solder joints at left most and right most columns show the most crack compared to other columns. In addition, the cracks initiate from solder joint inner side (b) and propagate towards opposite side (a). These observations are in agreement with modeling results.

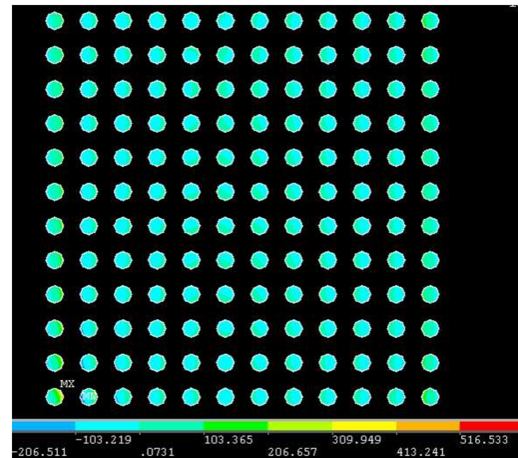


Figure 6. Stress distribution of corner WLP (group A). The mounting screw is located at lower left corner of the WLP. The mounting hole is located near package lower left corner.

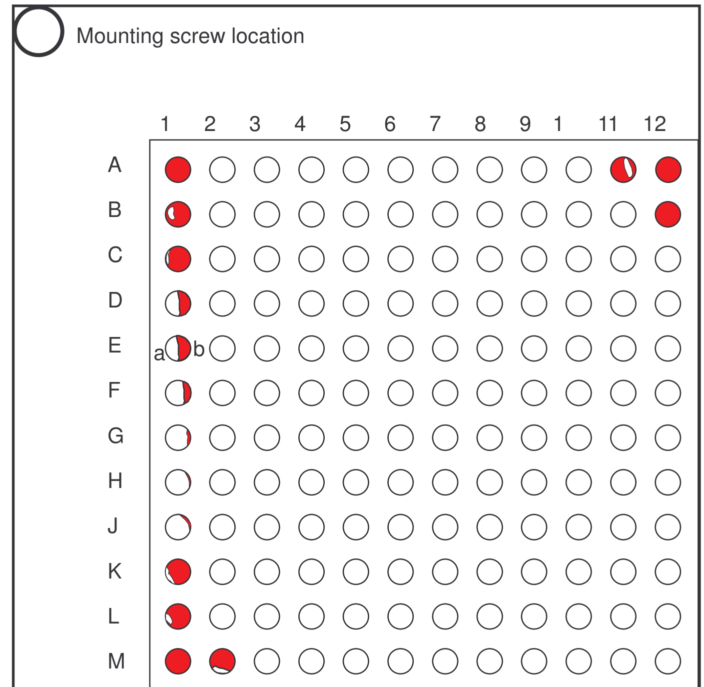


Figure 7. Crack map of a group A WLP after drop test. Red area corresponding to solder joint IMC crack at WLP side.

The maximum peeling stresses for all six component groups are plotted in Figure 8 for 12x12 and 6x6 array WLP. It is seen that sequence of groups from highest to lowest maximum peeling stress is A, F, E, B, D, and C. Therefore the drop test failure rate is expected to be A>F>E>B>D>C. The

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corner components (group A) see the highest stress and should fail first. Groups F and E are the next ones to fail. And B, C, and D have lower failure rates.
To verify this rating, drop test failure data for all six groups are plotted in Figure 9. Total of 10 test boards are considered in this case so to have sufficient failure data points for all groups. The failure rate trend is: A>F>E>B>D>C, which is in agreement with modeling. It is seen that group A (corner components) have the greatest failure rate. Groups C and D have smallest failure rates. When standard sample size of four boards is used, components in groups C and D often do not fail after significant number of drops. Failure rates of groups F, E, and B are in the same range. It is proposed to use characteristic life (CL) of data combing these three groups to represent the drop test reliability. This will be further elaborated.

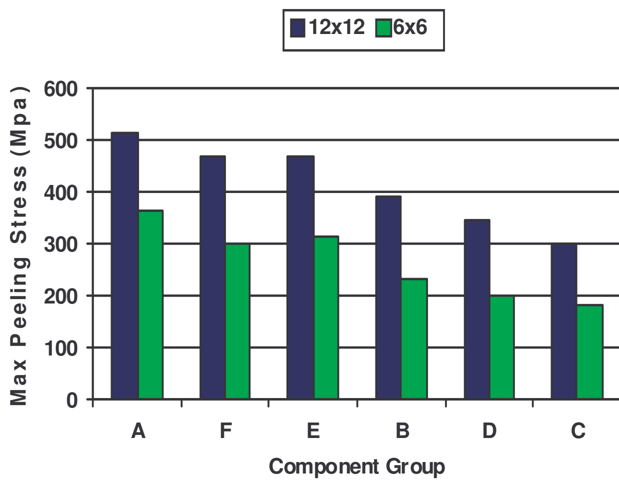

Figure 8. Maximum peeling stress at IMC at WLP side for a 0.5 mm pitch, 12x12 array WLP. The component groups are defined by Figure 1.

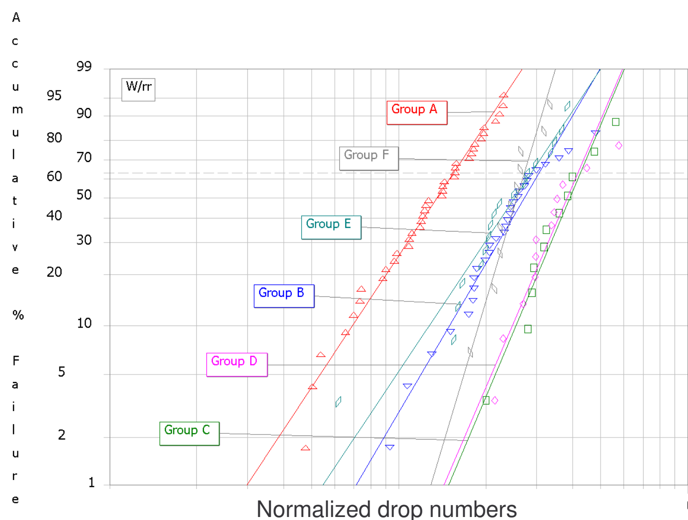

Figure 9. Weibull plots for six component groups. Groups B, E and F have similar failure rates.

For BGA packages, typically group A (corner) components fail much later than groups F and E (middle components)[11]. WLP failure pattern is different from BGA. In order to understand this difference, further investigation is conducted through FE modeling. Figure 10 shows the strain of the PCB during drop test. It is seen that there is very large strain and strain gradient next to the mounting screw. The closer the component is to mounting screw, the larger the solder joint peeling stress and therefore greater drop test failure rate. This indicates that the large failure rate of group components is mainly due to the effect of the mounting screws.

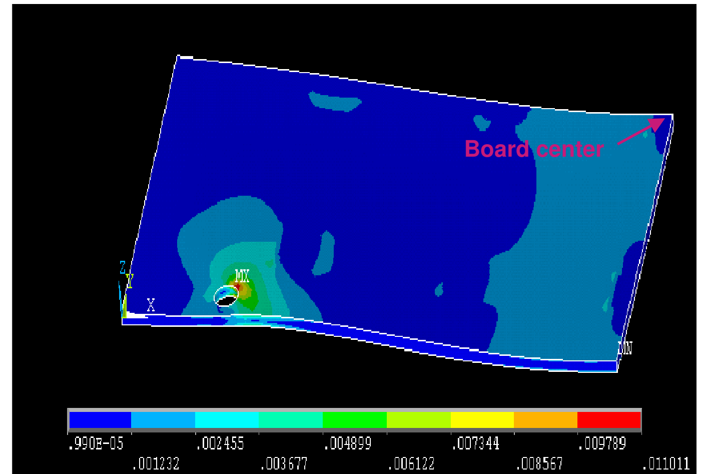

Figure 10. Von Mises strain plot of the drop test board. Only one quarter of the board is modeled due to symmetry.

To further verify, drop test with a PCB using different component placements were conducted while keeping the same drop test board outline. The corner components were placed 6 mm further away from the mounting holes in x and y directions. It is found that group A components now fail later than groups E and F. The drop CL for group A is increased by 2.2x due to the increased distance between the WLP and mounting screw (Figure 11). This verifies again that group A high failure rate is due to effect of mounting screws.

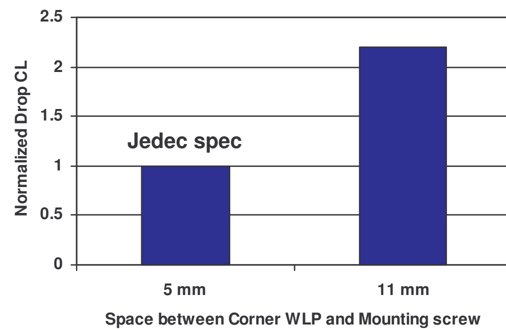

Figure 11. Effect of spacing between mounting hole and corner WLP component.

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It should be pointed out that component placements different from JEDEC specification are employed by some researchers while JEDEC type drop test boards are used. This results in different drop test reliability readings. Direct comparison of the drop test reliability data obtained from assemblies with different component placement is misleading.

To investigate alternative way to eliminate the failure due to mounting screws, additional drop test modeling is done but with different PCB approach[14]. With this approach, component locations stay the same, while the PCB size is increased by 4 mm in both length and width directions (Figure 12). The mounting holes are therefore moved 2 mm farther away from corner component in both directions compared to JEDEC standard board. The comparison of maximum peeling stress is given by Figure 13.

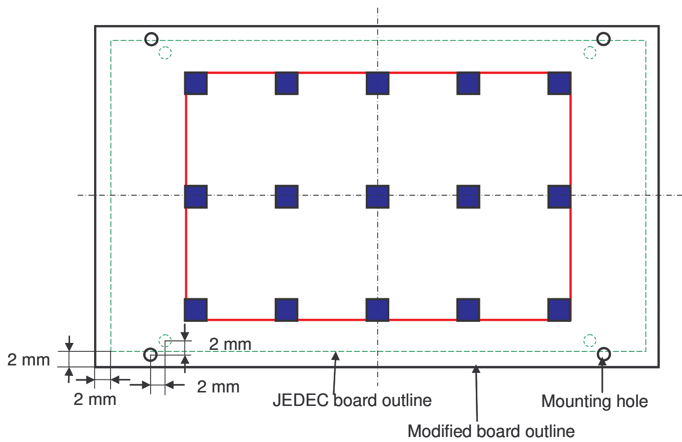

Figure 12. Illustration of modified drop test board. Mounting holes are moved 2 mm further away from corner components. Drawing not to scale.

It is seen from Figure 13 that when the modified board is employed, the maximum solder joint peeling stress of group A components is reduced by 33% compared to the standard JEDEC board. While the difference for groups B, E, and F is less than 5%. This verifies that the corner component drop test reliability is very sensitive to its distance to the mounting screws. The fact that the corner component group A always show highest failure rate for the WLP drop test using JEDEC boards is mainly due to the effect of the mounting screw not due to the intrinsic drop reliability of the package. Therefore, it is not appropriate to judge the WLP drop test reliability using data of corner components (group A).

In this study, combined data of groups B, E, and F are used to represent the drop reliability of WLP. To simplify the comparisons, normalized CL for group B, E, and F components are used for the subsequent discussions.

The effects of PCB layout, WLP structures, array size, pitch, and solder ball metallurgy are presented next.

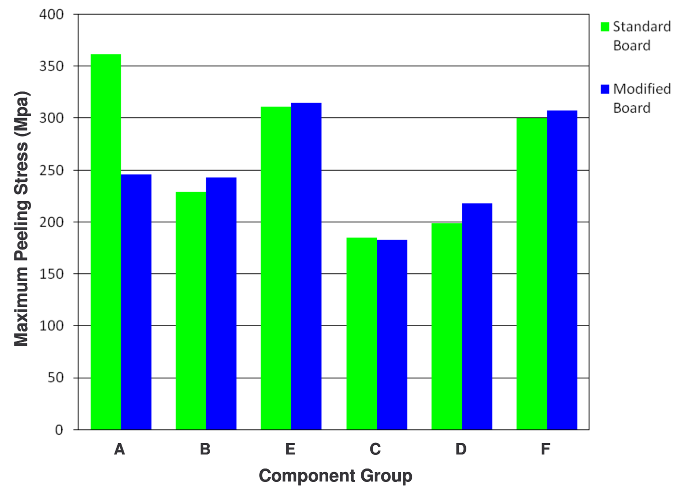

Figure 13. Maximum peeling stress for JEDEC standard drop test board and modified boards. 6x6 array WLP is considered in this study.

EFFECT OF PCB PAD DESIGN

JESD22-B111 recommends the 280 µm non-solder mask defined (NSMD) pad for 0.5 mm pitch BGA. The PCB pad size for 0.5 mm pitch WLP is typically 220 to 250 um. It is of interest to understand the effect of PCB pad design. Drop tests for 0.5 mm pitch WLP are conducted using PCB's with three pad designs: 250 um NSMD, 250 um SMD, and 280 um NSMD. The CL of these three cases are plotted in Figure 14 with 250 um NSMD as baseline. It is seen that the drop test reliability is dropped by 19% by using SMD pad, and it is dropped by 5% when for 280 um NSMD. Therefore it is concluded that NSMD pads gives better drop test reliability than SMD pads. NSMD pad size does not make significant difference. PCB with 250 um NSMD will be used as baseline for the subsequent discussion for 0.5 mm pitch WLP.

For SMD pad PCB, fracture of IMC at PCB side is also seen. The mixed failure modes result in higher failure rate.

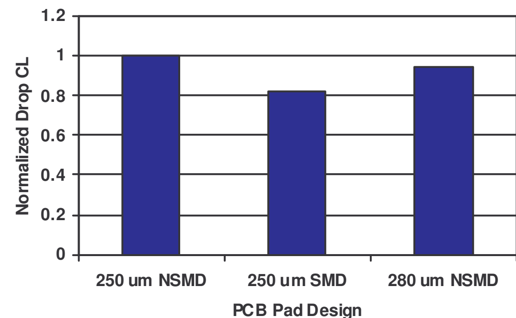

Figure 14. 0.5 mm pitch WLP drop test life as a function of PCB pad design.

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EFFECT OF WLP STRUCTURE CHIOCE

In this study three different WLP structures are considered. They are labeled as WLP A, B, and C. The CL comparison of these WLP structures is shown in Figure 15. It is seen that WLP B and C have approximately the same CL. While WLP A has the best solder joint reliability at drop with approximately 2.5x CL compared to WLP B and C.

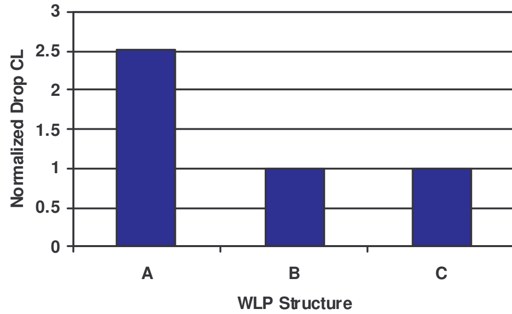

Figure 15. Drop test life comparison among three different WLP structures.

EFFECT OF WLP BALL PITCH

Drop test CL of 12x12 array 0.5 and 0.4 mm pitch WLP are shown in Figure 16. The results incorporate the test results for multiple WLP structures. For a given ball array, 0.4 mm pitch WLP CL is reduced by 14% compared to 0.5 mm pitch. The CL drop is probably due to the reduction of UBM side and solder joint diameter reduction.

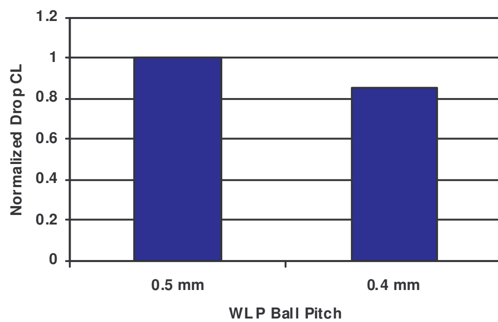

Figure 16. Drop test life comparison between 0.5 and 0.4 mm pitch WLP.

EFFECT OF BALL ARRAY SIZE

The comparison among these array sizes is given in Figure 17. It is seen that the CL drops exponentially as array size increases.

At this point it is of interest to compare the modeling results shown in Figure 8 where the maximum peeling stress increase from 6x6 to 12x12 array is 41%. While the drop test CL is reduced 85%. This implies that when a Coffin-Manson equation is used for empirical correlation, the exponent is approximately 5. This will be verified by further experimental data.

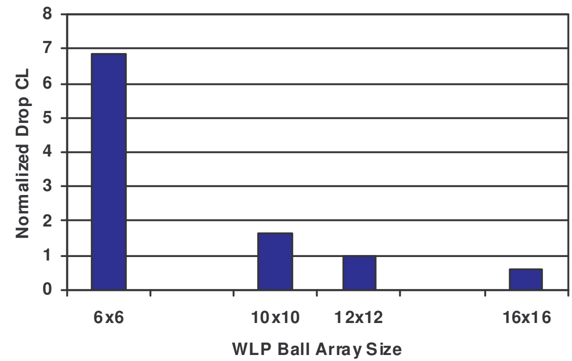

Figure 17. Drop test life comparison among different array sizes.

EFFECT OF SOLDER BALL ALLOY

Three solder ball alloys are studied through drop test. The CL comparison is shown in Figure 18. It is seen that choice of solder ball alloy has significant effect on drop test reliability and it can make a difference up to 30%.

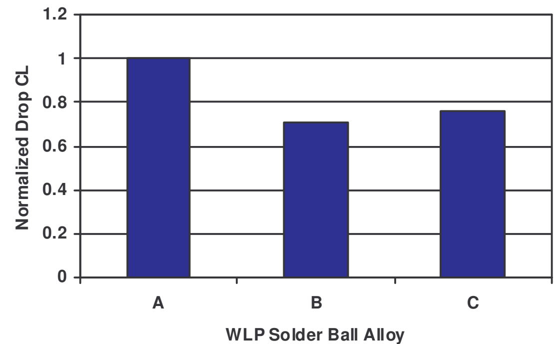

Figure 18. Drop test life comparison for three solder ball alloys considered.

CONCLUSIONS

In this study, large array WLP drop test reliability is studied with drop test experiments and modeling. Effects of board design, WLP structures, array size, ball pitch and solder ball materials are studied. It is concluded that:

1. For standard JEDEC drop test, group A WLP fail first. The high failure rate of group A is mainly due to the effect of mounting screws rather than the intrinsic strength of the package. It is not appropriate to judge the drop test reliability of a WLP with failure rate of group A WLP. Instead, combined data for groups B, E, and F should be used to compare WLP drop test reliability.

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2. For a given WLP, corner balls always fail first during drop test. The crack initiates at inner side of the solder joint and propagate towards the opposite side.
3. NSMD PCB pad gives better drop test reliability than SMD pad.
4. WLP structure A gives the best drop reliability. Choice of WLP structure makes visible difference.
5. With a given ball array, WLP with smaller pitch has worse drop reliability.
6. Drop reliability significantly decreases with array size increase.
7. Solder ball alloy choice makes significant difference in drop reliability. Solder alloy A give the best drop reliability among the three considered.

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